We claim:

1. A board, comprising:

a transmitter; and

an equalizer to automatically determine a multi-tap equalization setting based on loss of a link coupled to the transmitter.

2. The board of claim 1, wherein the equalization setting is a two-tap equalization setting.

3. The board of claim 1, wherein the equalization setting is a five-tap equalization setting.

4. The board of claim 1, further comprising:

receiving a signal which includes link loss information through a predetermined channel.

5. The board of claim 1, further comprising:

a look-up table to store a plurality of tap coefficient settings in correspondence with a respective number of link loss values, the equalizer searching the look-up table for a tap coefficient setting which corresponds to the link loss.

6. The board of claim 1, wherein the equalizer determines the equalization setting during link initialization.

7. The board of claim 1, wherein the equalizer receives information indicative of voltage and timing margins of an eye diagram at a receiver and adjusts the equalization setting based on the voltage and timing margins.

8. A method, comprising:

measuring loss in a link between a transmitter and a receiver; and

automatically determining a multi-tap equalization setting for the transmitter based on the measured loss.

9. The method of claim 8, wherein the equalization setting is a two-tap coefficient setting.

10. The method of claim 9, wherein the equalization setting is a five-tap coefficient setting.

11. The method of claim 8, wherein measuring the loss is performed at the receiver.

12. The method of claim 11, wherein measuring the loss includes:

transmitting a clock signal from the transmitter to the receiver; and

computing the loss as a ratio of the transmitted clock signal amplitude and the received clock signal amplitude.

13. The method of claim 12, wherein the receiver receives the clock signal through an input which is offset calibrated.

14. The method of claim 13, wherein the receiver sweeps the offset to determine the amplitude of the received clock signal to within a predetermined error.

15. The method of claim 14, wherein the predetermined error is one LSB error.

16. The method of claim 14, wherein the loss is measured based on the following equation:

$$\text{Loss (dB)} = -20 \log (N_{AC}/N_{DC})*(Vdc\_eq/V_{swing})$$

where N_{AC} is a number of steps to determine the amplitude of the received clock signal, N_{DC} is a number of steps to determine a voltage swing of a DC voltage transmitted to the receiver, Vdc_eq is an equalized DC voltage, and V_{swing} is the voltage swing.

17. The method of claim 8, further comprising:

storing a look-up table that includes a plurality of tap coefficient settings in correspondence with a respective number of loss values, wherein determining the equalization setting includes searching the look-up table for a tap coefficient setting which corresponds to the measured loss and setting an equalizer in the transmitter based on the tap coefficient setting obtained from the search.

18. The method of claim 17, wherein measuring the loss and determining the multi-tap equalization setting are performed during link initialization.

19. The method of claim 8, further comprising:

measuring voltage and timing margins of an eye diagram at the receiver; and

tuning the multi-tap equalization setting based on the voltage and timing margins.

20. A system, comprising:

a first circuit;

a second circuit; and

a data link connecting the first and second circuits,

wherein at least one of the first and second circuits includes:

(a) a transmitter, and

(b) an equalizer to automatically determine a multi-tap equalization setting based on a measured loss of the data link.

21. The system of claim 20, wherein the first circuit includes a chipset and the second circuit includes a CPU.

22. The system of claim 20, wherein the first circuit includes a chipset and the second circuit includes a memory.

23. The system of claim 20, wherein the memory is one of a RAM and a cache.

24. The system of claim 20, wherein the first circuit includes a memory and the second circuit includes a CPU.

25. The system of claim 20, wherein the first circuit includes a graphical interface and the second circuit includes at least one of a memory, CPU, and chipset.

26. The system of claim 20, wherein said at least one of the first and second circuits include:

a look-up table to store a plurality of tap coefficient settings in correspondence with a respective number of link loss values, the equalizer searching the look-up table for a tap coefficient setting which correspond to the link loss.

27. The system of claim 20, wherein the equalizer determines the equalization setting during link initialization.

28. A computer-readable medium storing a program to control equalization in a board, said program including:

a first code section to search a look-up table based on loss of a link connected to the board, said table storing a plurality of tap coefficient settings in correspondence with a respective number of loss values; and

a second code section to adjust an equalizer based on a tap coefficient setting generated from the search.

29. The computer-readable medium of claim 28, wherein the second code section adjusts the equalizer based on the tap coefficient setting during link initialization.

30. The computer-readable of claim 28, further comprising:

a third code section which tunes the equalization setting based on voltage and timing margins of a receiver eye diagram.